

Parylene Deposition

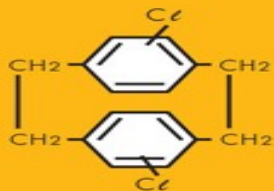
Nathan Jackson

April 2026

Parylene (deposition (polymer CVD))



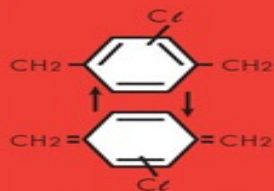
Dimer



Dimer, in powder form is added to the machine and heated to 150°C and changed to a vapour state.

stage 1

Monomer



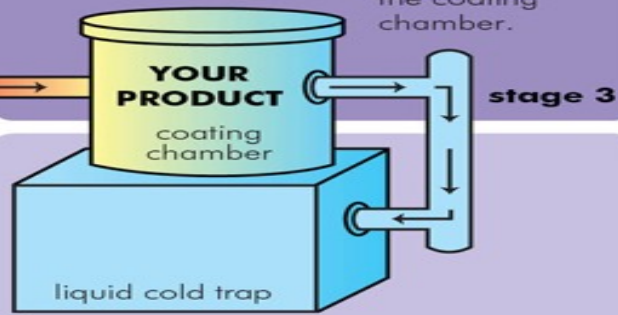
Next, the Dimer molecule is heated to 690°C, 0.5 torr. This changes the molecular structure to a monomer.

stage 2

Polymer

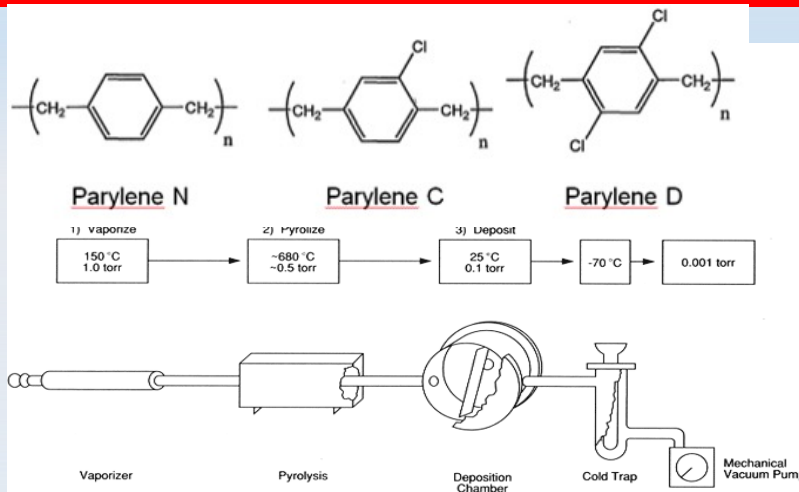


At room temp, the monomer becomes a polymer, bonding to products placed in the coating chamber.

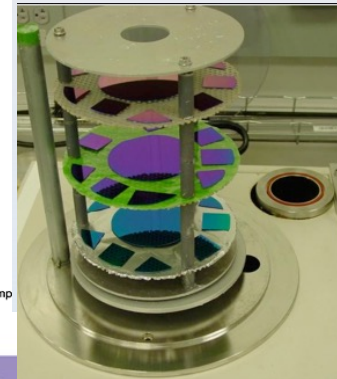


Excess process gas travels from the coating chamber into an external liquid cold trap.

stage 4



- Polymer deposited by CVD
- Pin hole free deposition (200nm-40um)



Parylene Applications

- Stent Coatings
- PCB or IC coating (moisture barrier)
- Biocompatible Coating
- MEMS
- Microfluidics
- Corrosion or Abrasion Protection
- Reduce Friction for catheters/needles
- Syringe coating
- Stretchable or Flexible Circuits
- Photonics Packaging (transparent properties)
- Organic LED's
- Fab process (shadow mask, acid/solvent protection layer, etc..)
- Coating for any Biomedical device
- ETC...

Parylene Properties

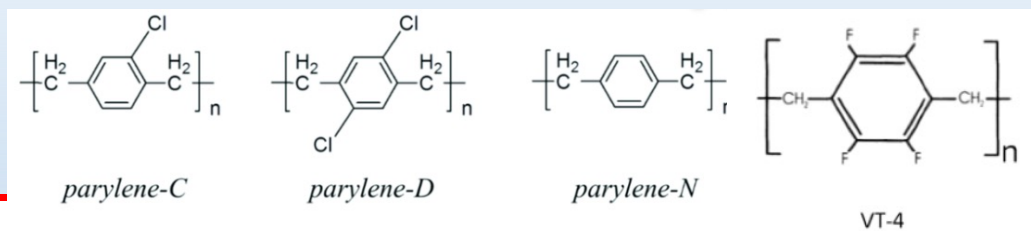


TABLE 5: Parylene Physical and Mechanical Properties

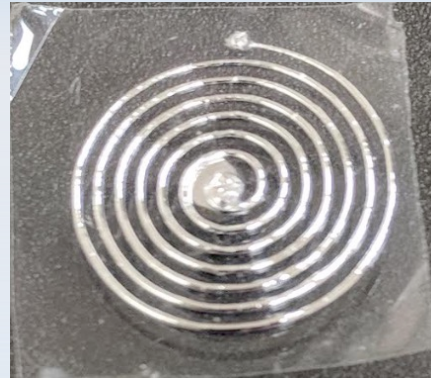
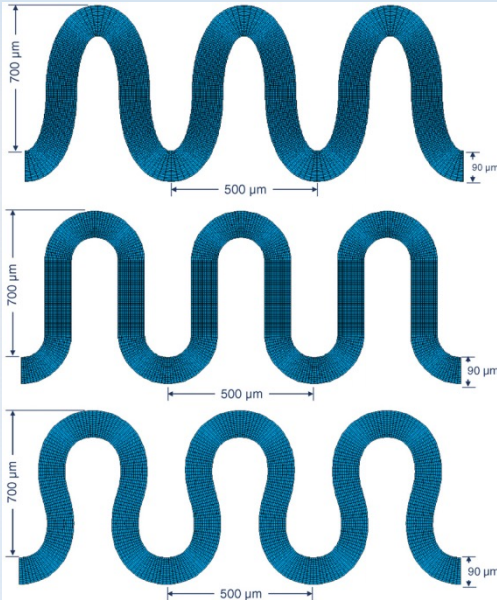
	Method	Parylene N	Parylene C	Parylene D	Parylene HT	Acrylic (AR) ^{a,b}	Epoxy (ER) ^{a,b}	Polyurethane (UR) ^{a,b}	Silicone (SR) ^{a,b}
Secant (Young's) Modulus (psi)	1, 2	350,000	400,000	380,000	370,000	2,000 – 10,000	350,000	1,000 – 100,000	900
Tensile Strength (psi)	3	7,000	10,000	11,000	7,500	7,000 – 11,000	4,000 – 13,000	175 – 10,000	350 – 1,000
Yield Strength (psi)	3	6,100	8,000	9,000	5,000	–	–	–	–
Elongation to Break (%)	3	Up to 250	Up to 200	Up to 200	Up to 200	2 – 5.5	3 – 6	>14	100 – 210
Yield Elongation (%)	3	2.5	2.9	3.0	2.0	–	–	–	–
Density (g/cm ³)	4	1.10 – 1.12	1.289	1.418	1.32	1.19	1.11 – 1.40	1.10 – 2.50	1.05 – 1.23
Index of Refraction (n _D ²⁵)	5, 6	1.661	1.639	1.669	1.559	1.48	1.55 – 1.61	1.50 – 1.60	1.43
Water Absorption (% after 24 hrs)	7	Less than 0.1	Less than 0.1	Less than 0.1	Less than 0.01	0.3	0.05 – 0.10	0.6 – 0.8	0.1

TABLE 4: Parylene Thermal Properties

	Method	Parylene N	Parylene C	Parylene D	Parylene HT	Acrylic (AR)	Epoxy (ER)	Polyurethane (UR)	Silicone (SR)
Melting Point (°C) ^a	1	420	290	380	>500	85 – 105 ^b	NA	~170 ^b	NA
T5 Point (°C) (modulus = 690 MPa)	2, 3	160	125	125	377	–	110	~30	~125
T4 Point (°C) (modulus = 70 MPa)	2, 3	>300	240	240	>450	–	120	–	~80
Continuous Service Temperature (°C)	–	60	80	100	350	82 ^b	177 ^b	121 ^b	260 ^b
Short-Term Service Temperature (°C)	–	80	100	120	450	–	–	–	–
Linear Coefficient of Thermal Expansion at 25°C (ppm)	4	69	35	38	36	55 – 205 ^{b,c}	45 – 65 ^{b,c}	100 – 200 ^{b,c}	250 – 300 ^{b,c}
Thermal Conductivity at 25°C (W/(m•K))	5, 6	0.126	0.084	–	0.096	0.167 – 0.21 ^{c,d}	0.125 – 0.25 ^{c,d}	0.11 ^{c,d}	0.15 – 0.31 ^{c,d}

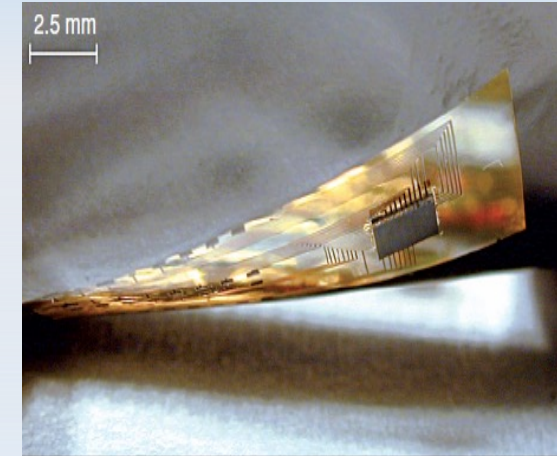
Very good Gas Barrier properties about 10,000x better than silicone

Interconnect design



Jackson et al 2018

Embedded Electronics



Cal tech 2007

Parylene balloon for MEMS actuation



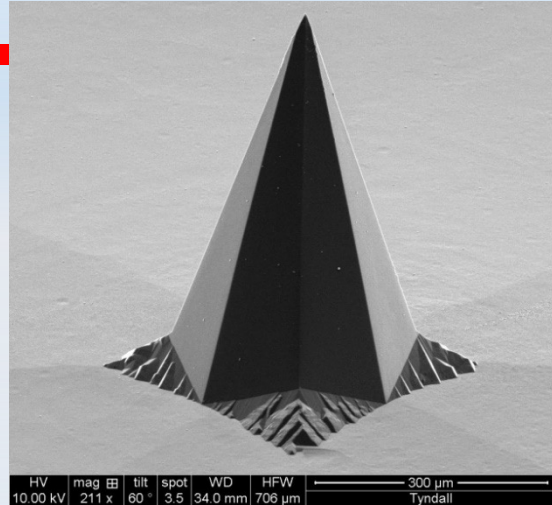
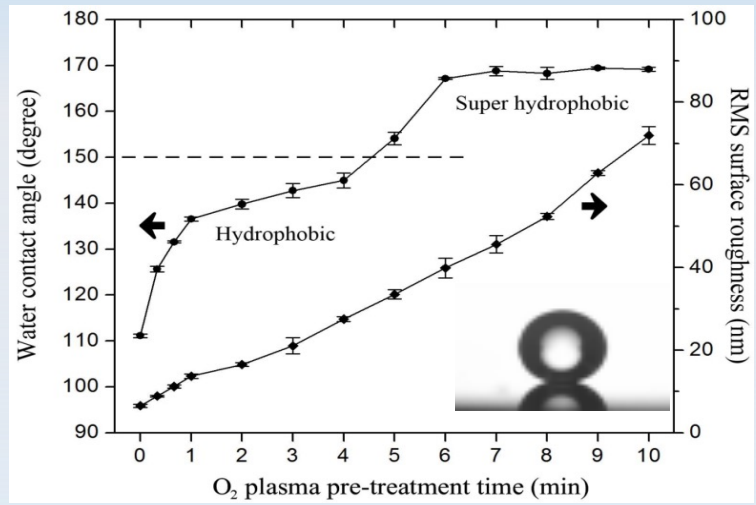
Cal tech 2006



Coatings

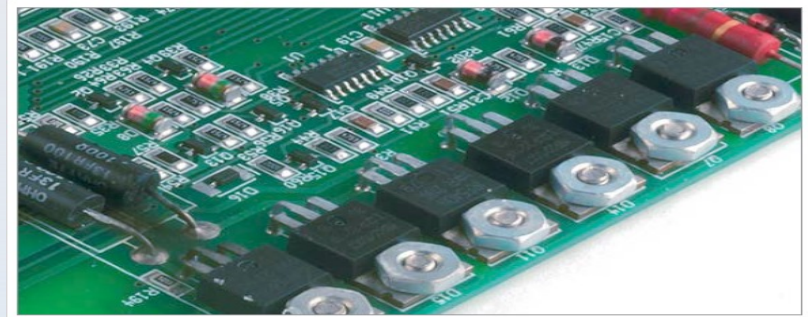
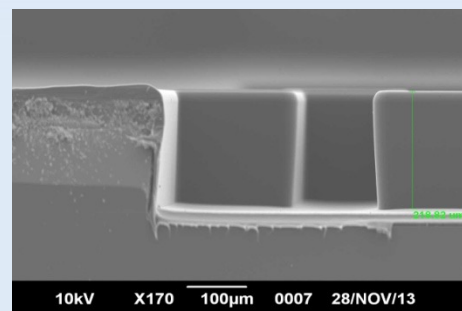
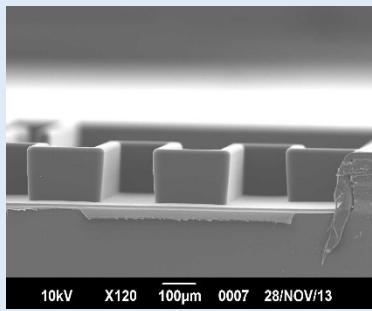
Coating of Micro-Needles

Parylene- into Super Hydrophobic Coating

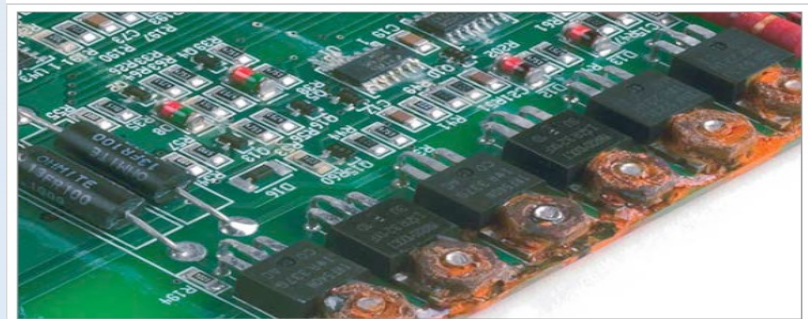


Jackson et al.

Transparent Polymer coating for 3D Micro structures



Coated with SCS Parylene HT

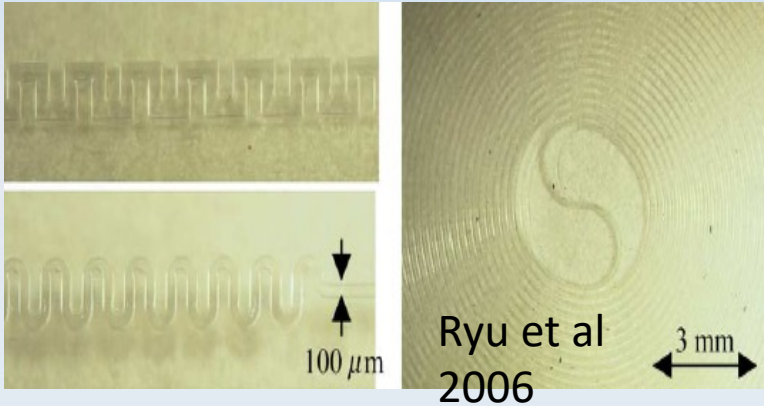


Uncoated

Coating of PCB as moisture barrier

Parylene Structures

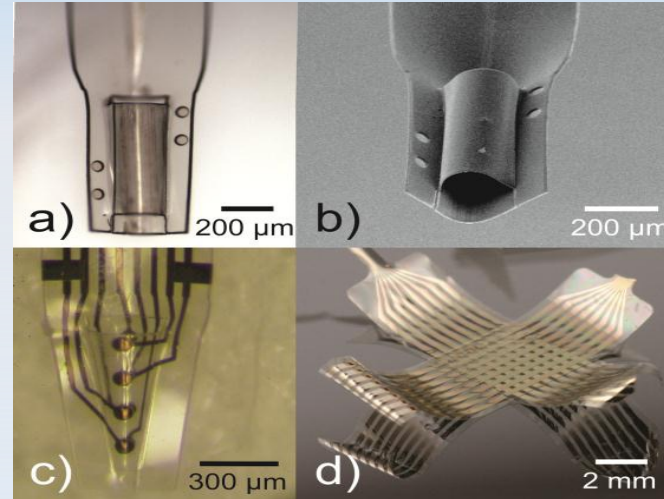
3D Microfluidic Channels



Shadow Mask Layer for Microfabrication



Thermoforming Neural Electrodes



Jonathan et
al. 2013

MEMS Cantilever for Energy Harvester



- ❑ Parylene is a polymer that is deposited using CVD (resulting in conformal pin hole free films)
 - ❑ Excellent moisture barrier, gas barrier, FDA compatible, transparent, flexible, somewhat stretchable, can handle elevated temperatures, and deposited at Room Temperature.

- ❑ If you have an application or want more information contact Dr. Jackson (njack@unm.edu)

Sputtering Deposition

AJA 5 target Sputtering System (workhorse)
Good for most applications

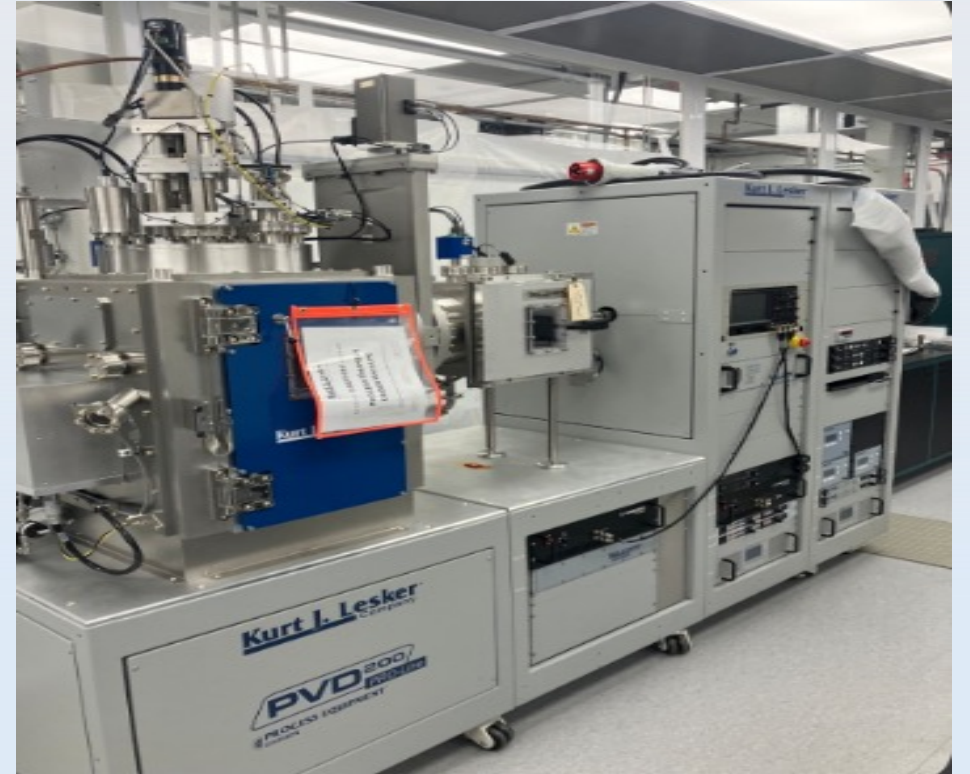


AJA Multi-gun Sputter system MTTC Plaza Photo 2021

Capabilities:

- 5 targets/guns
- Power source: DC, RF, Pulsed DC
- Substrate Temperature Control
- Reactive and Co-sputtering technology
- Materials
 - Single metals, dielectrics, some ternary materials (Al_2O_3 , ZnO etc...)

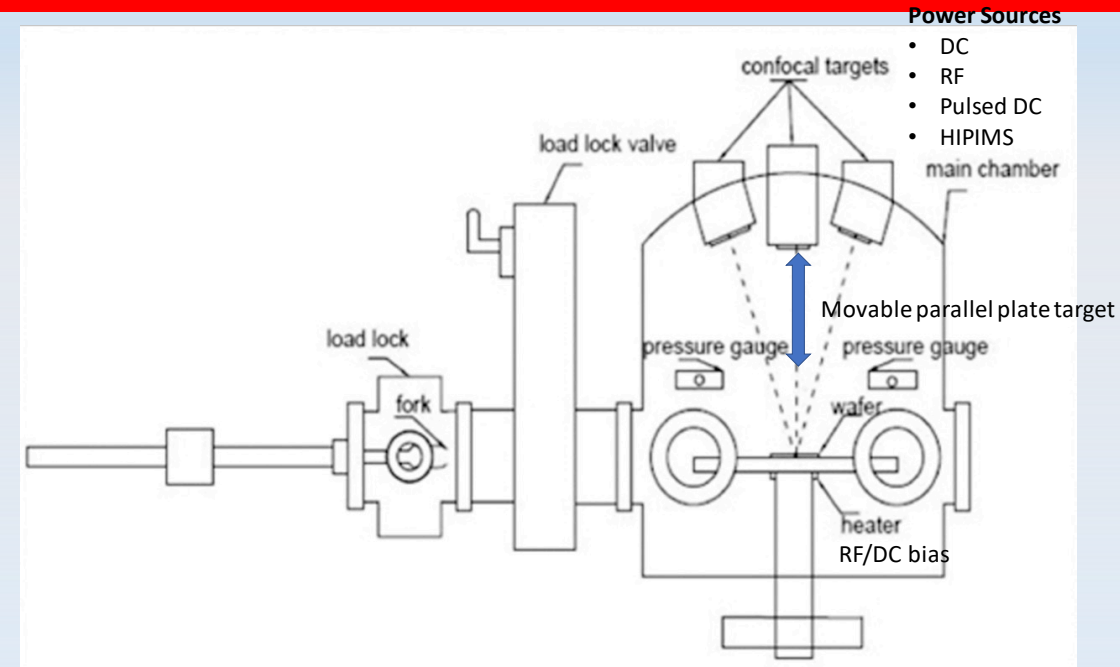
New SOA Custom Designed Sputter



- Tool was designed for Ternary or Quaternary Nitride Films
- Currently used for AlN and alloys

New Sputtering Tool Capabilities

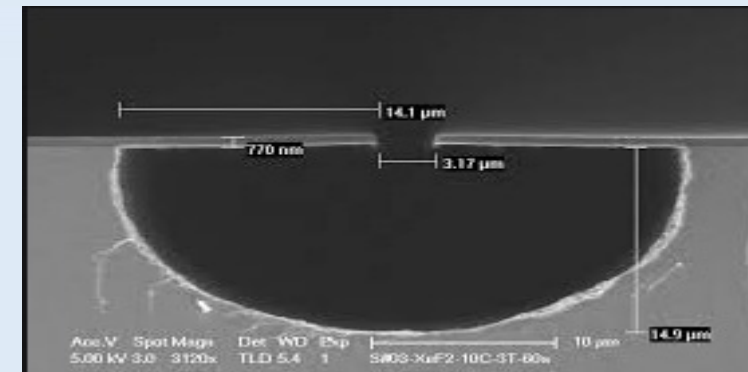
- ❑ Features of the New Sputter
 - ❑ Can handle up to 8" wafers
 - ❑ 4 confocal targets and 1 central target
 - ❑ Central target can alter target to substrate distance (to alter mean free path)
 - ❑ Power sources (2- DC, 2 RF, 2 Pulsed DC, and 2 HIPIMS (high power impulse magnetron))
- ❑ Temperature control (up to 800°C)
- ❑ RF Substrate Bias
- ❑ Ion Beam Etching (for pre-clean of wafer)
- ❑ Ultra high vacuum (base pressure $<1 \times 10^{-7}$ Torr)
- ❑ Integrated Ellipsometer (thickness measurements)
- ❑ Reactive Co-sputtering



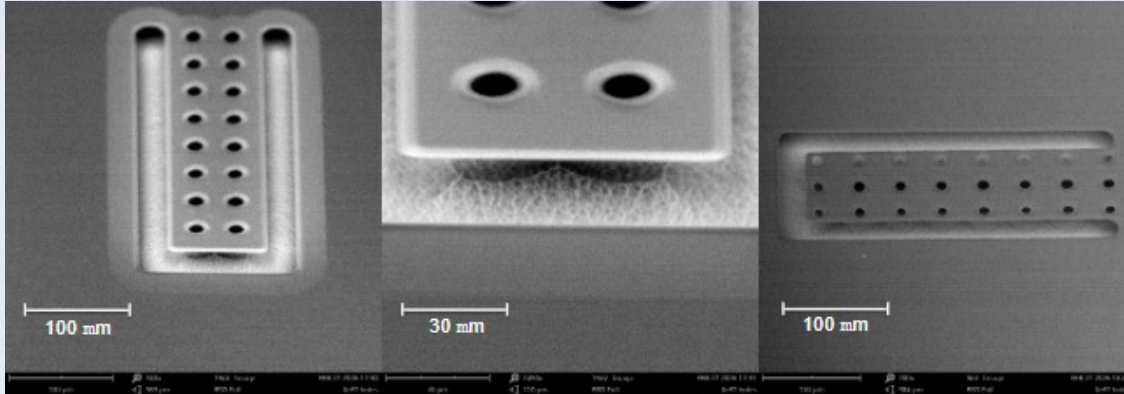
XeF₂ for Silicon Etching

XeF₂ Etching Basics

- ❑ XeF₂ is a non-plasma Gas etching process for performing Isotropic Etching of Silicon
- ❑ Etches:
 - ❑ Silicon, polysilicon, Ge and Mo (~ 1-10 μm/min)
 - ❑ Can also etch W, Ti, TiN, TiW (process not developed at MTTC yet)
- ❑ Excellent Selectivity
 - ❑ SiO₂ ~10,000:1
 - ❑ Does not etch photoresist, Al, Cr, AlN, Al₂O₃, PDMS, etc...

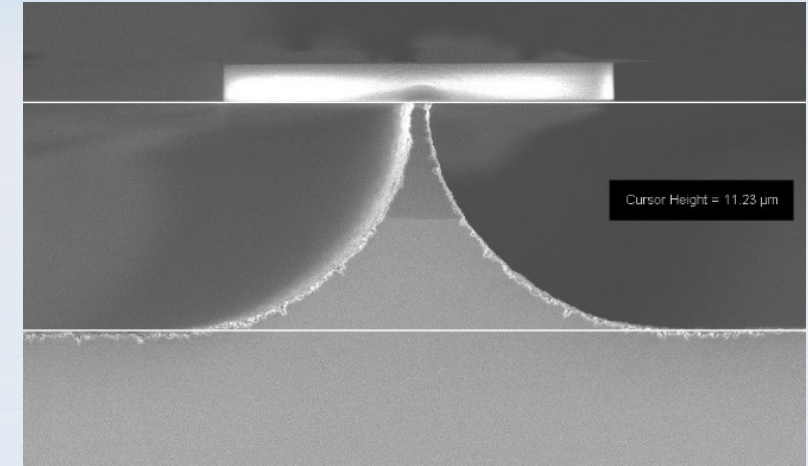


Cantilever Release

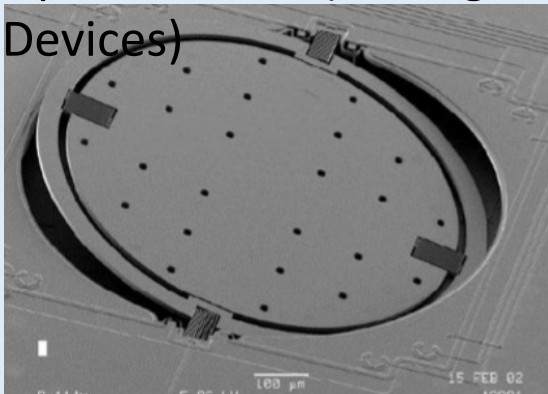


Trung et al 2026 (UNM)

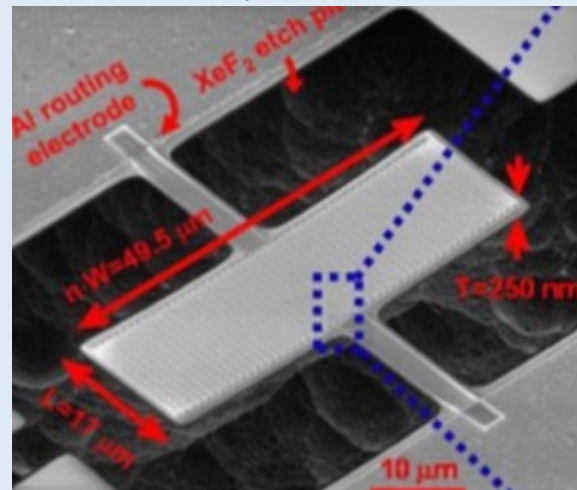
Needles or AFM Tips



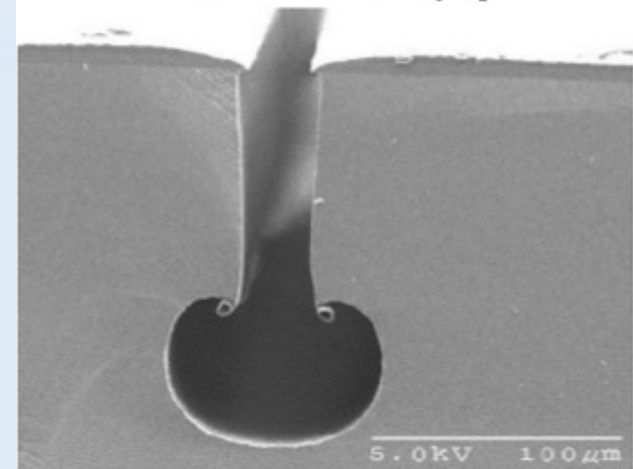
Optical Mirror (Analog Devices)



RF MEMS (Gianluca U. Penn)



Cooling Tubes, C₄F₈ Mask

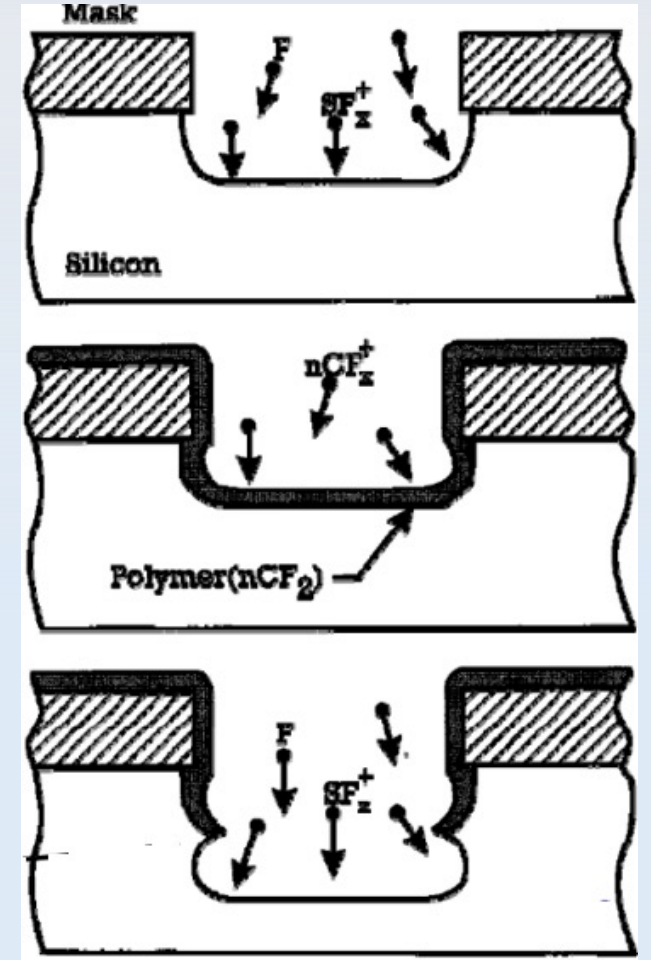


Carnegie Mellon University

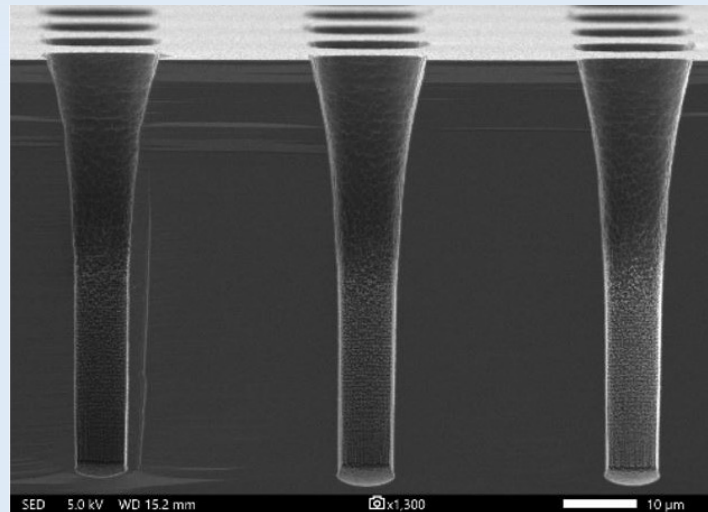
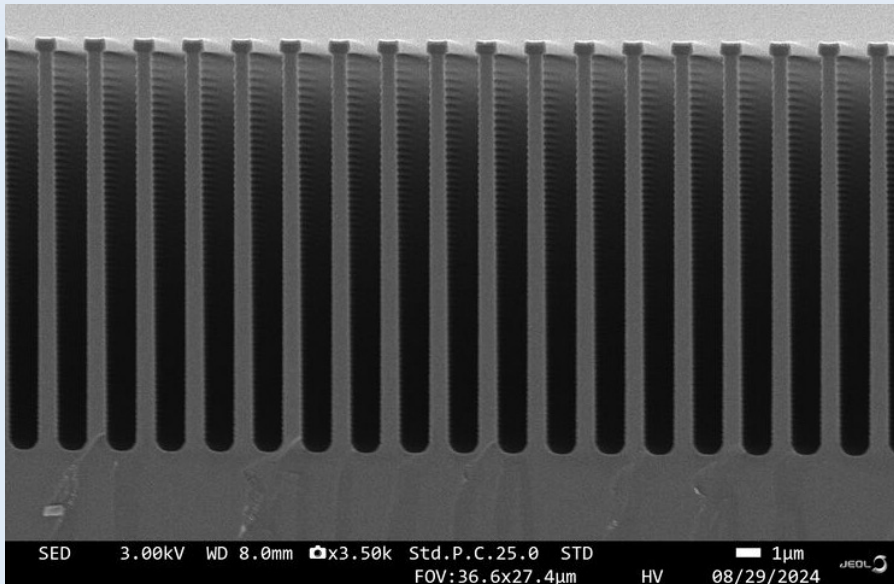
Deep Reactive Ion Etching (DRIE) aka Bosch Process for Silicon Etching

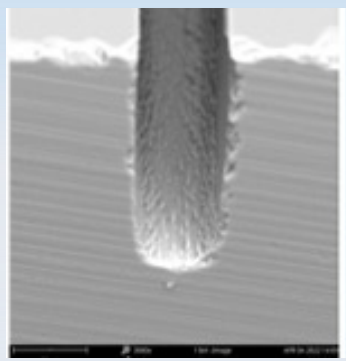
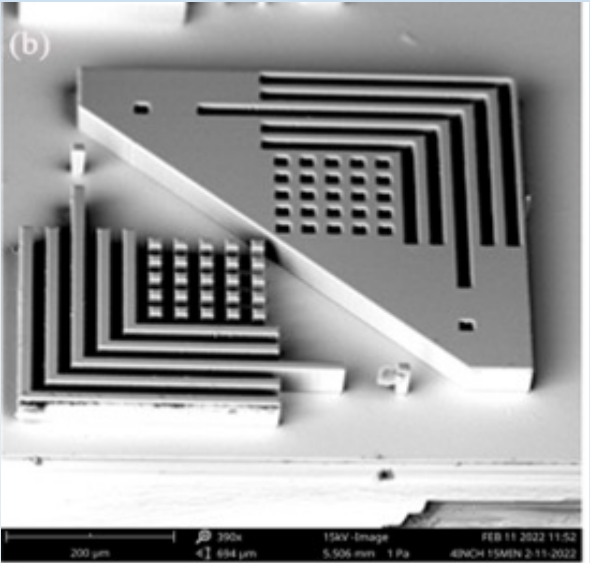
DRIE Etching Basics

- ❑ Invented in Mid 90's for etching thick films of Si (Anisotropic near 90° side wall)
- ❑ Uses High Density Plasma
- ❑ Alternates between etch cycle and depositions cycle
 - ❑ SF_6 (etching) and C_4F_8 (passivation)
- ❑ Good selectivity to SiO_2 , Nitride, or Photoresist (100:1)

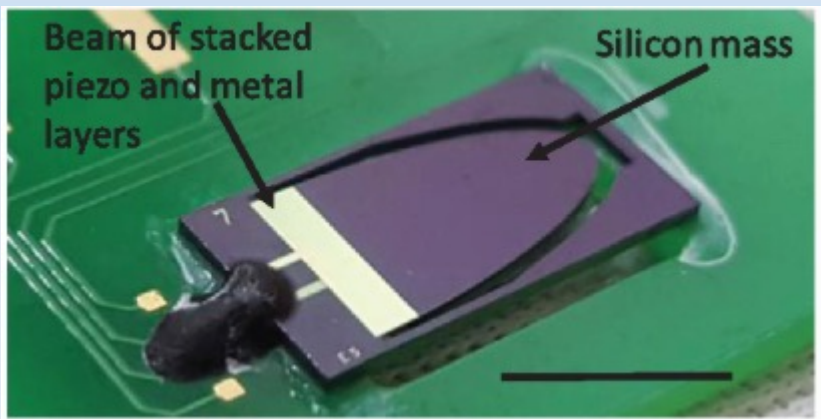


Through Silicon Vias channel formation

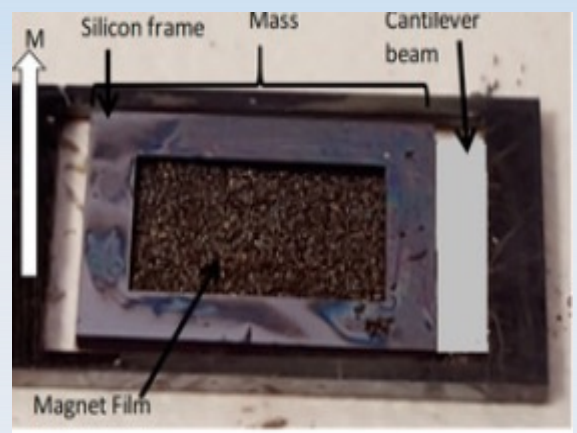




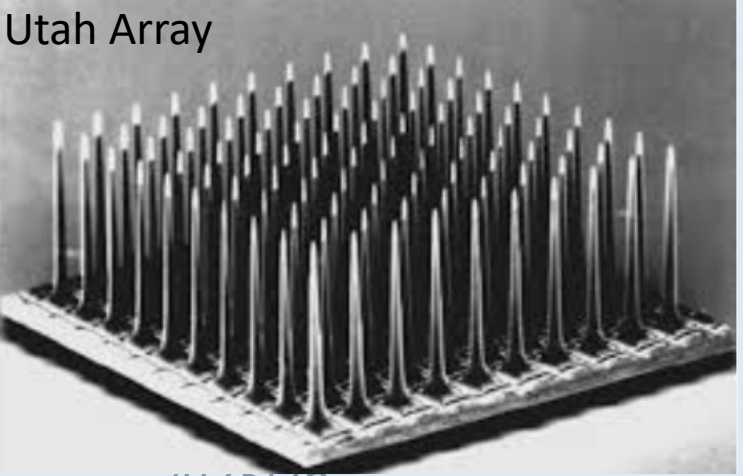
Pallavi et al 2022
(UNM)



Jackson et al (2018) Energy harvester
(Pacemaker)

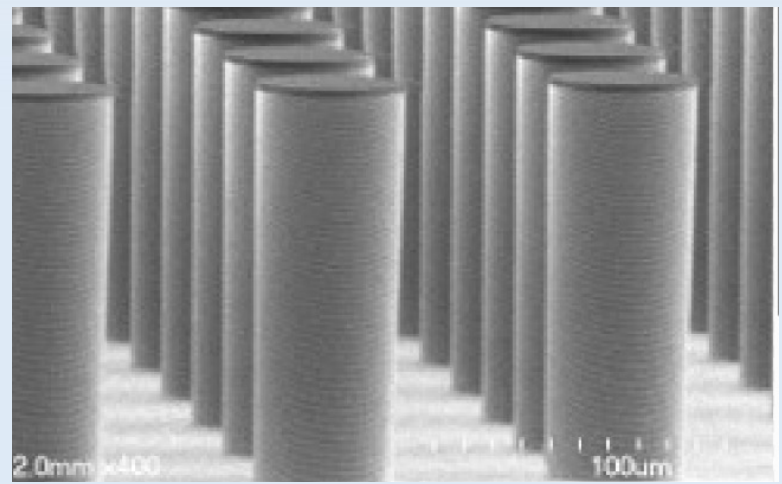


Implantable Neural Electrodes
Utah Array

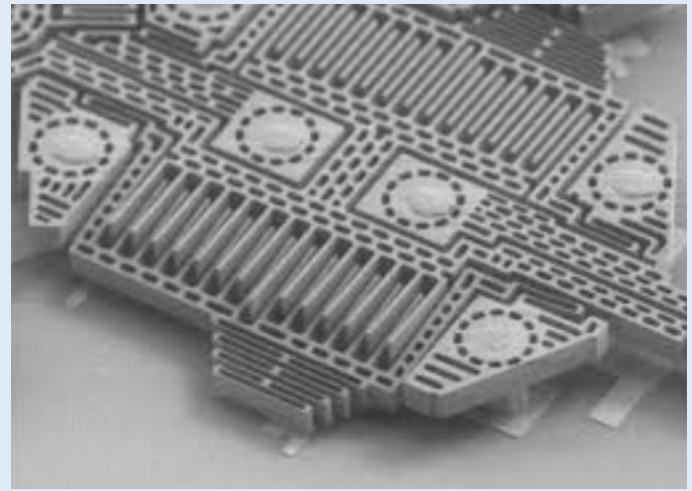


4/25/20

Pillars and Phononic Crystal Waveguides



Resonators



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